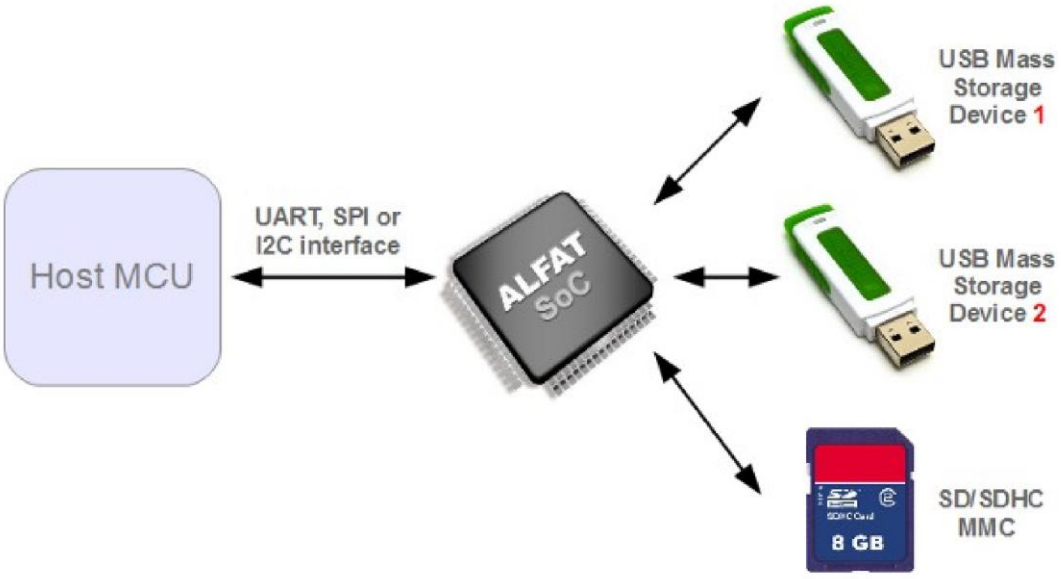
GHI Electronics, LLC
501 E. Whitcomb Ave.
Madison Heights, Michigan 48071
Phone: (248) 397-8856
Fax: (248) 397-8890
www.ghielectronics.com

Preliminary F40 SoC Datasheet



Where Hardware Meets Software

1 Contents

2 Introduction

The F40 SoC (previously known as ALFAT) is a small, low cost, and low power hardware file system solution. Through the F40 SoC, simple commands are used to access files on USB drives and SD, SDHC, and MMC memory cards. The F40 SoC can also read keystrokes from keyboards. Commands can be transmitted over UART, SPI, or I2C.

Throughout this document, the F40 SoC will be referred to as the F40. For detailed command descriptions and device behavior, please the file system user manual.

For advanced electrical characteristics and details on the underlying STM32F205RBT6 processor, please consult the processor's datasheet.

2.1 Key Features

- Serial UART, SPI, and I2C command interfaces
- File reading, writing, and deleting
- Long File Name support
- FAT16 and FAT32
- Access up to 16 files simultaneously
- USB storage device support
- Built in 2x USB 2.0 Full Speed PHY
- Support for one High Speed ULPI USB PHY
- 4-bit SD/MMC storage support
- SD-Reader mode for accessing SD cards through USB
- Up to 4 Mbytes/s file access speed on SD and USB High Speed
- Up to 1 Mbytes/s file access speed on USB Full Speed
- Quick file-close pin for closing files on power loss
- Read keystrokes from USB keyboards
- Simulate an SD card reader
- Built in RTC with a separate power domain
- LQFP64 10 x 10 mm
- 40 mA run and as low as 0.1 µA sleep
- -40°C to +85°C operational
- RoHS Lead Free

2.2 Example Applications

- Data loggers
- Automated machinery
- Consumer products

3 Pinout Table

Any pin with no function or note must be left unconnected. All I/Os are 5 V tolerant except the reset pin.

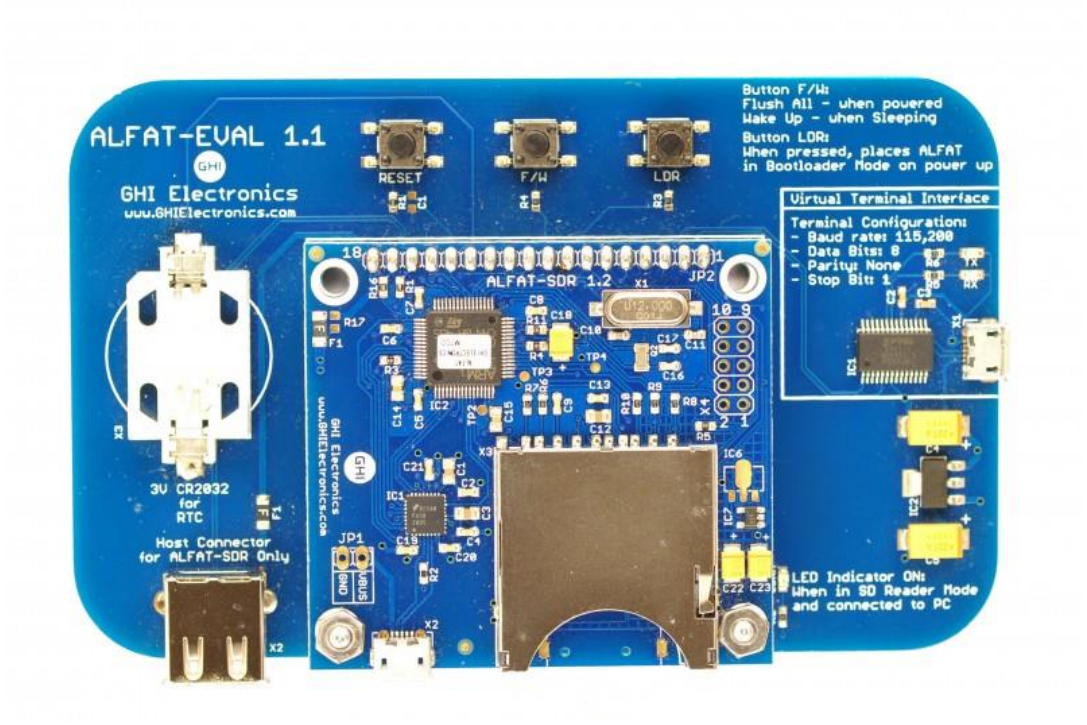
Pin	Function	Pin	Function
1	VBAT	33[3]	USB1 ULPI D5
2		34[3]	USB1 ULPI D6
3	RTC XTAL IN	35[7]	USB1 D-
4	RTC XTAL OUT	36[7]	USB1 D+
5	SYS XTAL IN	37	
6	SYS XTAL OUT	38	
7[1,2,9]	RESET	39[8]	SD D0
8[3]	USB1 ULPI STP	40[8]	SD D1
9		41[3]	USB1 ULPI 19.2 MHz
10[3]	USB1 ULPI DIR	42	UART TX / I2C SDR CONNECT
11[3]	USB1 ULPI NXT	43[9]	UART RX / SPI BUSY / I2C BUSY
12	GND	44[10]	USB0 D-
13	3.3 V	45[10]	USB0 D+
14[11]	WAKEUP / FLUSH	46	
15		47[6]	
16		48	3.3 V
17[3]	USB1 ULPI D0	49	
18	GND	50[11]	SPI SSEL
19	3.3 V	51[8]	SD D2
20	DATA READY	52[8]	SD D3
21[3]	USB1 ULPI CK	53	SD CLOCK
22	SPI MISO / UART BUSY	54[8]	SD COMMAND
23[11]	SPI MOSI	55[2,12]	SPI CLOCK / BAUD CONTROL
24[4]	SD WRITE PROTECT	56	
25[2,4]	SD CARD DETECT	57[3,9]	USB1 ULPI D7
26[3]	USB1 ULPI D1	58	I2C SCL / UART SDR CONNECT / SPI SDR CONNECT
27[3]	USB1 ULPI D2	59	I2C SDA
28[5]		60	
29[3]	USB1 ULPI D3	61	
30[3]	USB1 ULPI D4	62	
31[6]		63	GND
32	3.3 V	64	3.3 V

[1]Not 5 V tolerant
[2]Active low
[3]Connect only if ULPI High Speed PHY is used
[4]Connect to GND if unused
[5]Requires a 10,000 Ω pull-down resistor
[6]Requires a 2.2 µF capacitor to GND
[7]No connect if a High Speed PHY is used, otherwise requires a 22 Ω resistor in series
[8]Requires a 47,000 Ω pull-up resistor
[9]Requires a 10,000 Ω pull-up resistor
[10]Requires a 22 Ω resistor in series
[11]Interally pulled low
[12]Interally pulled high

4 Reference Design

The ALFAT OEM board and ALFAT SDR board are excellent starting points and reference designs for the F40 in both default and SD-Reader mode. See the product catalog entries for more information and additional resources.

The ALFAT Evaluation Kit is the best way to start evaluating the F40. The kit includes an evaluation host board and the ALFAT OEM and the ALFAT SDR boards. The host board can be easily connected to any PC using the included USB cable. The included explorer software can be used for visualizing of the command set.



5 Device Startup

The F40 is held in reset when the reset pin is low. Releasing it will begin the system startup process.

There are two different components of the device firmware:

1. GHI Bootloader: initializes the system, updates the firmware when needed, and executes the firmware.
2. Firmware: responds to host commands and interfaces with the SD card.

Which component gets executed on startup is controlled by manipulating the command interface selection pins. See Command Interface for details. When the GHI Bootloader is not selected, the firmware boots using the interface selected.

When the firmware first executes, it will print a startup banner followed by a response with a result code of 00. This banner must be read and discarded before executing any commands.

6 Supported Commands

The F40 uses GHI Electronics's standard file-system solution command set. Please see the File System User Manual for detailed information. Commands not listed below are not supported.

Command	Function	Notes
I	Initialize Media	
O	Open File	
W	Write File	
R	Read File	
F	Flush File	
C	Close File	
P	Seek File	
Y	Tell File	
D	Delete File	
L	Fast Write	
?	Find File	
@	Initialize File and Folder List	
N	Get Next File	
A	Rename Files	
M	Copy File	
K	Free Size	
Q	Format	
T	Initialize Date/Time	
S	Set Date/Time	
G	Get Date/Time	
Z	Device Control	Z 0, Z 1, and Z 2 only
B	Set Baud Rate	
V	Version	
#	Echo Commands	
E	Test Media	
J	Get Status	

7 Command Interface Selection

To determine which interface to use, the F40 samples the SPI SSEL and SPI MOSI on power up. The interface continues to be the same until the device is reset or the power is cycled. Both SPI SSEL and SPI MOSI have internal pull down resistors. Leaving these pins unconnected will default the interface to UART. The GHI Bootloader always uses the UART interface.

Interface	SPI MOSI	SPI SSEL
UART	Low	Low
GHI Bootloader	High	Low
I2C	Low	High
SPI	High	High

8 Design Considerations

8.1 Required Pins

Exposing the command interface selection pins and the UART pins are required in every design to enable device programming, updates, and recovery.

8.2 Power Supply

A typical clean power source, suited for digital circuitry, is needed to power the F40. Voltages should be within 10% of 3.3 V. Decoupling capacitors of 0.1 µF are needed near every power pin. A large capacitor, typically 47 µF, should be near the F40 if the power supply is more than few inches away. Lastly, 22 µF or larger capacitors are needed near the SD card.

8.3 Crystals

The main system clock is provided through a 12 MHz crystal that is rated 500 ppm or better with a load capacitance of around 18 pF. The optional RTC crystal is 32.768 kHz with a load capacitance of around 12.5 pF.

8.4 Real Time Clock

The internal clock resets on power loss. The F40 can be provided with the proper time on power up or it can utilize the built in RTC. The RTC runs independently off its own power source and crystal. It is powered through the VBAT pin and requires 1.65 V to 3.6 V. In the case of a drained battery, a common cathode-dual-diode circuit needs to combine the power from the battery source and the main power into the VBAT pin.

8.5 USB PHY

Both USB ports have built in Full Speed PHYs. Only a 22Ω series resistor needs to be added on the USB bus lines.

An external USB High speed ULPI PHY can be added to F40. The Fairchild FUSB2805 is recommended. The F40 generates the 19.2 MHz clock needed by the PHY.

8.6 Performance

The brand, age, and quality of the media used greatly affects its performance. Continuously writing to the media also degrades its performance. The F40 does its best to buffer the data and only write to the actual media when necessary or when a file is flushed. Care must be taken when to flush the open files.

While the F40 fully supports FAT16 and FAT32, some media may not work. Reasons can include insufficient power, unstable power, the clock is too high, or the card does not completely comply with the standards.

8.7 Serial Interfaces

8.7.1 UART

The default baud rate is 115,200 with no parity, eight data bits, and one stop bit. The default baud rate for the firmware only (not the bootloader) may be changed on power up to 9,600 using the BAUD CONTROL pin. All signals are 3.3 V TTL levels. If RS232 is desired, adding an RS232 level shifter is required.

8.7.2 SPI

The maximum clock is 24 MHz, the clock idle state is low, data is sampled on the rising edge, data is sent MSB first, and SSEL is active low. There must be a 4 µS delay between each byte sent when sending the data with Write command.

8.7.3 I2C

The maximum clock is 400 kHz. The 7-bit I2C address is 0x52.

9 Legal Notice

9.1 Licensing

The F40, with all its built-in software components, is licensed for commercial and non-commercial use. No additional fee or licensing is required. Software, firmware, and libraries provided for the F40 are licensed for use on the F40 only.

9.2 Trademarks

F40 and ALFAT are a trademarks of GHI Electronics, LLC.

Other registered or unregistered trademarks are owned by their respective companies.

9.3 Disclaimer

IN NO EVENT SHALL GHI ELECTRONICS, LLC BE LIABLE FOR ANY DIRECT, INDIRECT, INCIDENTAL, SPECIAL, EXEMPLARY, OR CONSEQUENTIAL DAMAGES (INCLUDING, BUT NOT LIMITED TO, PROCUREMENT OF SUBSTITUTE GOODS OR SERVICES; LOSS OF USE, DATA, OR PROFITS; OR BUSINESS INTERRUPTION) HOWEVER CAUSED AND ON ANY THEORY OF LIABILITY, WHETHER IN CONTRACT, STRICT LIABILITY, OR TORT (INCLUDING NEGLIGENCE OR OTHERWISE) ARISING IN ANY WAY OUT OF THE USE OF THIS PRODUCT, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGE. GHI ELECTRONICS, LLC LINE OF PRODUCTS ARE NOT DESIGNED FOR LIFE SUPPORT APPLICATIONS. SPECIFICATIONS, AVAILABILITY, AND PRICE ARE SUBJECT TO CHANGE WITHOUT NOTICE.

10 Revision History

Revision	Date	Change
1.0	2016-06-16	Initial preview release.